Design of High Gain 2.4GHz CMOS LNA Amplifier for Wireless Sensor Network Applications

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***Abstract*— Wireless Sensors Networks (WSNs) are being widely deployed in various applications, such as in monitoring environment conditions and in security systems. However, the device size, low cost and low energy are the main problems in the design of WSNs. In this paper, a high gain CMOS LNA for 2.4 GHz WSN application is proposed and simulated in 0.18 um CMOS technology. A novel energy efficient technique along with the current bleeding PMOS devices is employed to improve both the NF and power gain of the LNA design. Furthermore, the folded cascade is improved by combining the Partial Source Degeneration (PSD), shunt feedback and boosting inductor. Simulation results show that the proposed LNA approach outperforms the conventional fold cascode LNA in terms of gain (S21) and NF. Also, the proposed LNA achieves a forward gain of 31 dB with a NF of 2.66 dB, while drawing 9.75 mW from a 1V source supply; and a linearity Input Third-Order Intercept Point (IIP3) of -2.5 dBm.**

Keywords— Wireless micro sensor nodes; current bleeding; 0.18um CMOS technology; Partial Source Degeneration PSD; boosting Inductors; Gain, Linearity.

I. INTRODUCTION

Wireless Sensor Networks (WSNs) have recently attracted a great attention in the research community. With a purpose of providing short range connectivity with significant fault tolerance, these systems are being applied in various areas, such as in environmental monitoring, industrial process automation and field surveillance. In practice, the low voltage, low cost, device size and high integration are the main challenges in the design of WSNs. In addition, these networks are battery dependent ones. Thus, the energy consumption of their receivers should be reduced as well as the receiver sensitivity must be maintained to get long lifetime [1, 3]. The basic WSNs topologies are shown in Fig. 1.

In practice, to enhance both the power consumption and lifetime of WSNs, CMOS technologies are deployed due to their low power, low cost, and high integration [2]. These technologies integrate the design of analog and Radio Frequency (RF) circuits in their platforms [2,4].

To that end, the Low noise amplifier (LNA) is the first component of the WSN RF receiver. Its main role is the amplification of the received weak RF signal with the minimum possible noise ratio from the antenna. In addition, it has a significant trade-off between gain, noise figure, input impedance matching, stability, linearity and power consumption. Practically, for narrowband LNA design, both the Common Source (CS) and Common Gate (CG) topologies are the most commonly deployed architecture topologies. [6 -15]

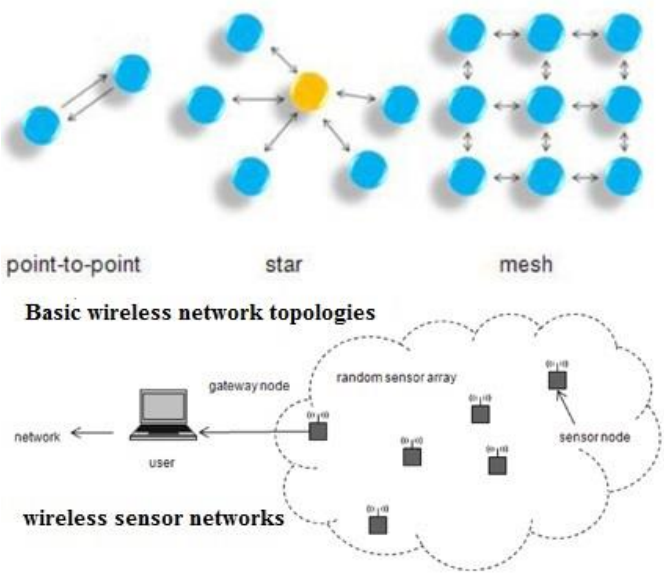

Fig.1. Wireless sensor network and topologies [1,3]

In this paper, fold cascode topology is used to more suitable for achieving high gain, low power consumption and low noise figure for WSN applications. The presented design is based on the combining the Partial Source Degeneration (PSD), shunt feedback and boosting inductor to meet the specifications of IEEE 802.15.4 (Zigbee) as it is becoming a popular choice for implementing wireless sensor networks [1]. Zigbee requires a minimum input-referred third order intercept point (IIP3) of -10dBm. However, the NF specification is relaxed since the proposed design intended for short-range applications, such as WSN.

The rest of the paper is organized as follows. Section II describes the noise canceling technique in LNA. Section III describes the proposed LNA circuit. Section IV provides the simulation results of the proposed LNA and Section V concludes the results of this work.

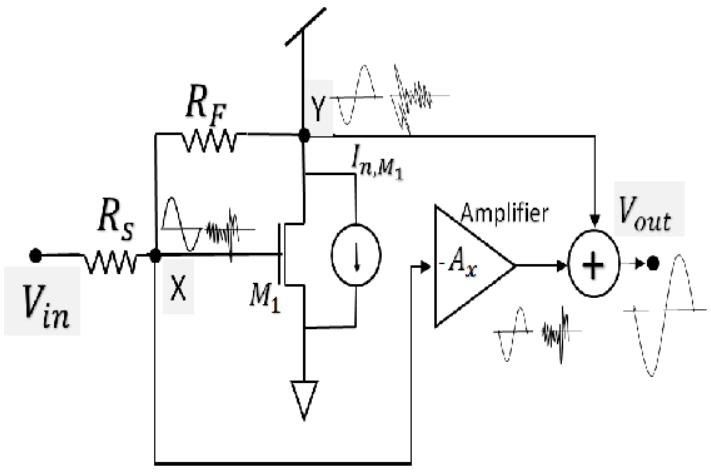

Fig.2. Simple resistive shunt feedback LNA with conventional noise cancellation technique [18]

II. Noise Canceling Technique in LNA

In practice, the noise cancellation technique is applied to produce noises with opposite phase-polarities in various paths and to cancel noises presented in the output. The application of this technique permits for simultaneously noise cancellation and impedance matching due to the irrelevance among the cancellation and input impedance. One of the main noise cancellation techniques is the conventional one. A simple resistive shunt feedback LNA with conventional noise cancellation technique is shown in Fig.2, [5, 11].

As shown above, the LNA includes a resistor R_f, an input transistor M_1 and a feedback voltage amplifier that has a specific gain A_x $(A_x > 0)$. The power transfer is maximized based on designing input impedance Z_{in} and matching it with the amplifier source impedance R_s. The value of Z_{in} is equal to $\left(\frac{1}{g_{m1}}\right)$, where g_{m1}stands for the transconductance of M_1.

Nonetheless, this expression is derived with if the loading impact at node Y is neglected. On the other hand, this condition does not ensure enhancing the NF. Thus, the noise of M_1 is modeled by a current source I_{n,M_1} among the source and drain in order to detect the noise at the output. This current source produces noise voltages at nodes X and Y; $V_{n,X}$ and $V_{n,Y}$ with similar phase polarity. But, the signals voltages at these nodes; V_X and V_Y have opposite phase polarities. Thus, the output noise voltage can be expressed as follows: [5, 12]

$$V_{n,out} = I_{n,M_1}\left(R_s + R_f - A_x R_s\right) \quad (1)$$

To have zero output noise voltage, the feed forward voltage amplifier gain must be:

$$A_x = 1 + \frac{R_f}{R_s} \quad (2)$$

Based on this expression, the noise of M_1 is canceled at the output. Furthermore, any noise current source, which flows among the source and drain of M_1 is canceled too. On the other hand, the achieved overall voltage gain A_V after canceling $V_{n,out}$ for the signal voltage can be computed as follows:

$$A_V = \frac{V_{out}}{V_X} = \left(1 - g_{m1}R_f\right) - A_x = -R_f\left(g_{m1} + \frac{1}{R_s}\right) \quad (3)$$

In practice, the cancellation is not based on the condition of input matching. Thus, $Z_{in} = \frac{1}{g_{m1}} = R_s$. In addition, A_V is equal to $-2\left(\frac{R_f}{R_s}\right)$ for simultaneous input matching and noise cancellation. Based on equations in (2) and (3), A_V is directly related to A_x, while A_x is in proportional relation with R_f. But, large values of R_f induce noises and decrease the bandwidth. In practice, the decrease in the bandwidth is unavoidable regardless of dividing R_f by A_V. Thus, in this paper, we have a tradeoff among the bandwidth and gain despite that both the noise cancellation and input matching are completed

III. Design of LNA

A. Shunt Feedback

The shunt feedback is one of topologies of the LNA architectures, which differ in the input matching. Fig. 3 illustrates the schematic resistive shunt feedback LNA and its equivalent RLC input matching network, [13, 15].

As shown in the Fig. 3, the input impedance at M_1 gate is transformed into a series network of both R_{ser} and C_{res}. The following formula expresses the C_{sc}:

$$C_{gs}\left(1 + \frac{1}{{Q_L}^2}\right), R_{series}\frac{R_f + R_L}{\left(1 + g_m R_L\right)\left(1 + {Q_L}^2\right)} \quad (4)$$

The R_L represents the output impedance $\frac{L_L}{C_L}$ at a specific operating frequency, where it can be expressed as follow:

$$Q_L\frac{\omega_0 LG}{R_{series}} \quad (5)$$

The voltage gain at M_1 is boosted by the series matching topology about $(1 - jQ_L)$. Thus, the efficient transconductance is boosted about $\left(1 + {Q_L}^2\right)$. The LNA can then achieves a voltage gain by $\sqrt{\frac{\left(1+{Q_L}^2\right)}{{Q_L}^2}}$.

B. Current Bleeding

The current bleeding technique is mainly applied to enhance the conversion gain. A simple current bleeding diagram is shown in Fig. 6. This technique is added mainly among the switching and transconductance stages to offer a solution for inconsistency of both noise and linearity, reduce the bias current at the switching stage and maintain the bias current at the transconductance stage. In addition, it enhances the input current with no effect on the switching stage and the load current. The enhancement in the switching stage current

enhances the noise performance because of the low noise pulse height, [2, 9].

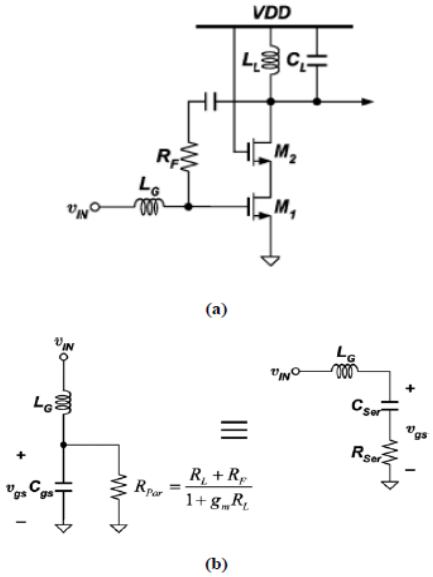

Fig.3. Schematic resistive shunt feedback LNA and its equivalent RLC input matching network [2]

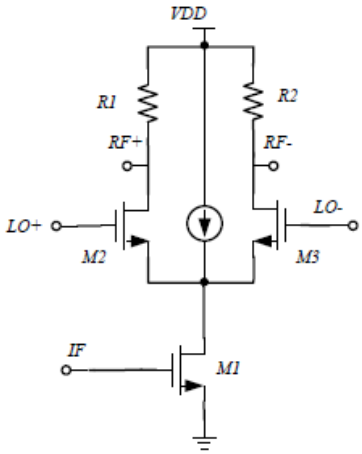

Fig.4. Simple current bleeding diagram [2]

C. *Designed LNA Structure*

In this work, the design of the LNA starts by setting the length of the transistor to the minimum possible value and using the metric presented in [14, 16] to find the best width. The fundamental principle of this metric is that both the total gain and power consumption are the only two effective parameters on the energy efficiency. Thus, the general energy-efficiency metric can be expressed as follows:

$$Efficiency\ (E) = f(Gain, Power) = \frac{log(gain)}{power} \qquad (6)$$

A folded-cascode structure is used to reduce the power consumption and enhance the linearity of the proposed LNA.

Fig. 5 shows the proposed LNA design based on a cascode (CS-CG) with shunt feedback and external CS stage cascading with CB stage to offer high gain.

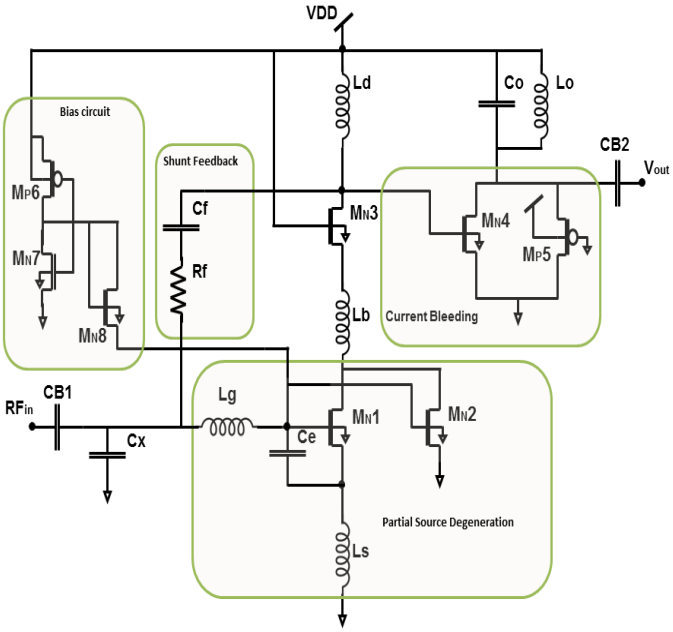

Fig. 5. The proposed 2.4GHz schematic LNA

As shown in the figure above, both transistors; M_{N1} and M_{N2} are CS configurations. These two transistors are cascode common source amplifiers that use the same supply current to reduce the DC current consumption. In addition, they are cascoded with M_{N3} transistor using the current reuse to save the DC current. The transistor M_{N4}, which cascaded with M_{N3}, is used to increase the power gain. Thus, the total DC gain for this circuit is expressed as follows:

$$A_v = \frac{(g_{m1} + g_{m2})g_{m3}}{g_{d2}g_{d3}} \qquad (7)$$

In order to increase the choke isolation, the L_b Mutual Coupled Degenerated resonant tank is employed. In addition, the boosting transistorM_{N2} is used to improve the input match with partial degenerate source, enhance the linearity and increase high reverse isolation. Both the resistive and capacitive shunt feedback; R_f and C_f are employed to improve both the stability factor and input impedance matching.

The transistors M_{P6}, M_{N7} and M_{N8} form a CMOS voltage divider to provide bias voltage to the gate of the amplifier. In addition, a choke inductor in parallel with a tank capacitor forms a resonant tank, where this in turn increases the choke isolation. To mitigate the inductive degeneration term, Ce capacitor is used in parallel with the CS capacitor of the transistor. The new input impedance can be obtained from the equivalent impedance of the circuit shown in Fig. 5. Thus, the equivalent input impedance can be expressed as follows:

$$Z_{eq} = \frac{Z_{cgs1}Z_{cgs2}}{Z_{cgs1} + Z_{cgs2}} + Z_{ls} + g_{m2}Z_{cgs2}Z_{ls} \quad (8)$$

So, it can be expressed as the resonant frequency as follows:

$$Z_{eq} = \frac{\frac{1}{\omega C_{gs1}}\left(\omega(L_s \pm M) - \frac{1}{\omega C_{gs2}}\right) - j\frac{R_x}{\omega C_{gs1}}}{R_x + j[\omega(L_s \pm M) - \frac{1}{\omega C_{gs1}} - \frac{1}{\omega C_{gs2}}]} \quad (9)$$

where: R_{in} is a real partition controlled by the degenerated transistor. Thus, Z_{eq} becomes dependent on the g_{m2} as expressed below:

$$R_{in} = R_x = \frac{g_{m2}(L_s \pm M)}{C_{gs2}} \quad (10)$$

Then, extra capabilities are presented to adjust the circuit input impedance, besides the increase in the gain. However, there is a tradeoff between NF and gain of the amplifier. Thus, the increase in the gain results in a decrease in the NF [2, 5, 13]. So, improving the gain improved the NF too. Also, there is compromise to increase IIP3 due to:

$$IIP3 \propto (V_{gs2} - V_{th2}) \mapsto I_D \propto \frac{W}{L}(V_{gs2} - V_{th2})^2 \quad (11)$$

Thus,

$$IIP3 \uparrow \Rightarrow (V_{gs2} - V_{th2}) \uparrow \Rightarrow I_D \uparrow \Rightarrow (L_s - M) \quad (12)$$

The main noise sources in a CMOS transistor are the thermal noise, flicker noise, noise presented in the resistive poly gate, noise resulted from the distributed substrate resistance and shot noise associated with the leakage current of the drain source reverse diodes. The most important noise when operating at high frequency is the thermal one, which can be calculated using the following formula [2, 13]:

$$i_d^2 = 4KT\gamma g_m \quad (13)$$

The noise factor of the cascade LNA can be computed using the formula below:

$$F = 1 + \frac{R_1}{R_s} + \frac{Rf}{Rs} + \frac{Ct^2}{Cgs^2}\frac{\omega^2 R_s(g_{m1} + g_{m2})\gamma}{\omega_T^2 \alpha}.x \quad (14)$$

where

$$x = \frac{\delta\alpha^2}{5\gamma}[1 + Q_s^2]\frac{C_{gs}^2}{C_t^2} + 1 - 2|c|\frac{C_{gs}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}} \quad (15)$$

and the quality factor Q_s is expressed as follows:

$$Q_s = \frac{1}{\omega_\circ R_s C_t} \quad (16)$$

and the correlation coefficient c in equation (15) is represented by:

$$c = \frac{\overline{i_{ng}^* i_{nd}}}{\sqrt{\overline{i_{ng}^2}\,\overline{i_{nd}^2}}} \quad (17)$$

To that end, a bias voltage must be chosen. For cascode LNA, the supply voltage should be greater than twice of a threshold voltage. However, the PMOS transistor Mp5 is used as a current bleeding device to allow a portion of current to flow through the current bleeding branch and consequently reduces the current that flows through the circuit. Thus, this technique can reduce the bias current and hence reduces the power consumption and improves the gain:

IV. EXPERIMENTAL RESULT

The proposed LNA is designed and simulated using TSMC 0.18μm CMOS technology at 2.4GHz in ADS. The S-parameters provides useful performance measures for the proposed LNA, such as the gain (S21), NF, reverse isolation (S12) and input return loss S11. In addition, the voltage gain is an important performance measure of the LNA, where it is calculated using the following formula:

$$Gain(dB) = 20Log\left(\frac{Vout}{Vin}\right) \quad (18)$$

In the proposed design, the gain value is increased by inter-stage matching inductor Lb and third stage MN4 at low bias voltage. Results presented that the proposed LNA achieved 31 dB of voltage gain. Fig. 6 shows the voltage gain of the proposed LNA.

The achieved NF is at a desired frequency as shown in Fig. 7. Based on this figure, the circuit has NF of 2.66 dB.

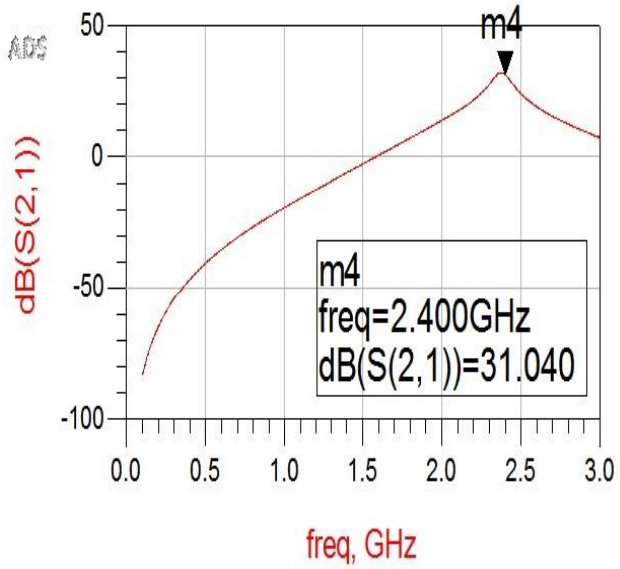

Fig.6. Forward Gain S21

As shown in Fig. 8, an IIP3 of -2.5 dBm at 2.4 GHz is obtained. This graph was created based on the two tones technique.

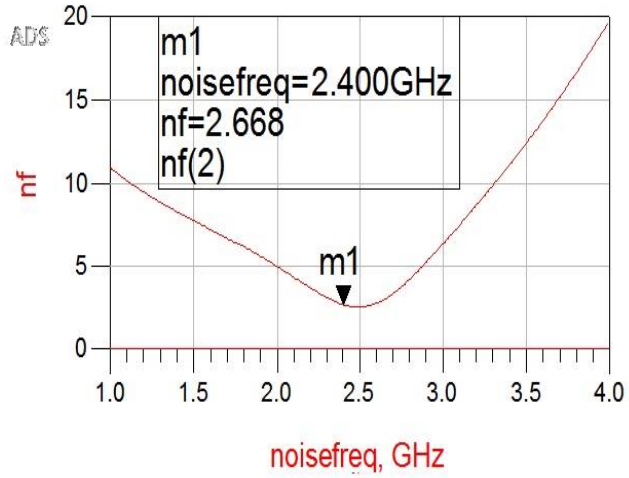

Fig.7. Noise Figure

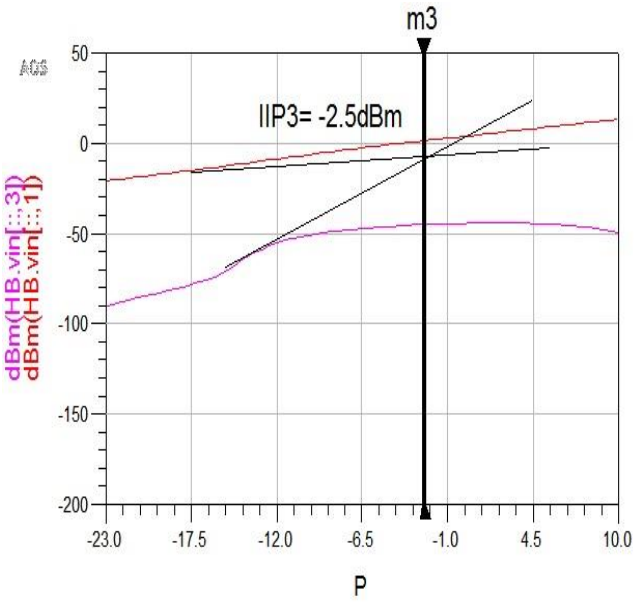

Fig.8. IIP3 versus input power

V. Conclusion

A 2.4GHz shunt feedback two-stage cascode LNA with interstage resonance technique is designed and simulated in 0.18µm CMOS technology. The presented LNA offers a sufficient gain for WSN applications. It has a gain of 31 dB and NF of 2.66 dB. It consumed 9.75 mW at a supply voltage of 1V. The proposed LNA is useful for low power WSN applications.

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